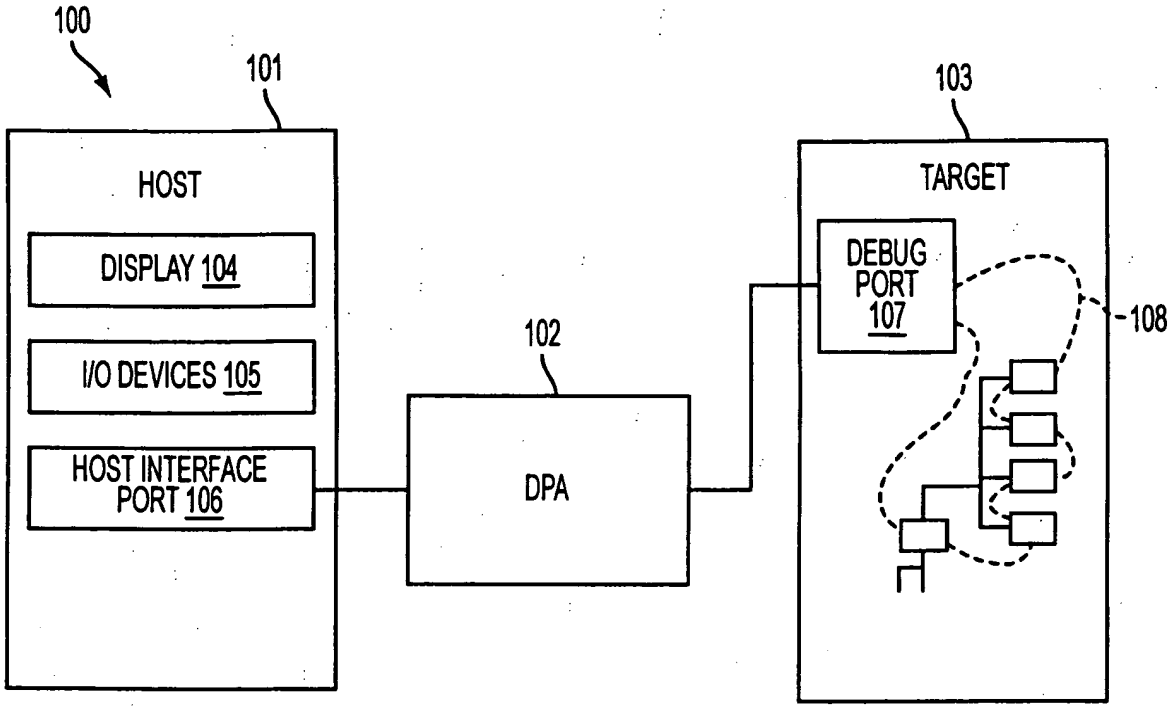
100
101
HOST
DISPLAY 104
I/O DEVICES 105
HOST INTERFACE PORT 106
102
DPA
103
TARGET
DEBUG PORT 107
108

FIG. 1

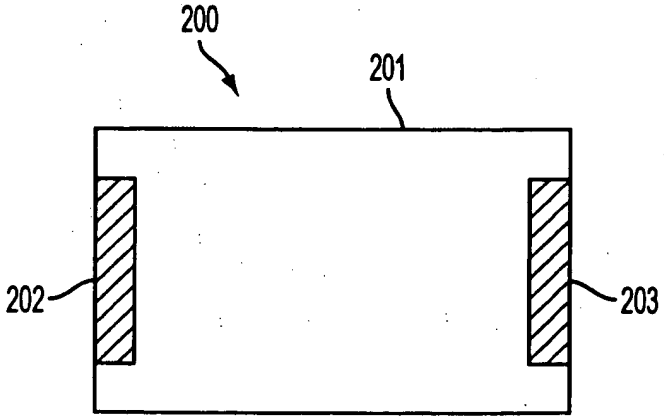
200
201
202
203

FIG. 2

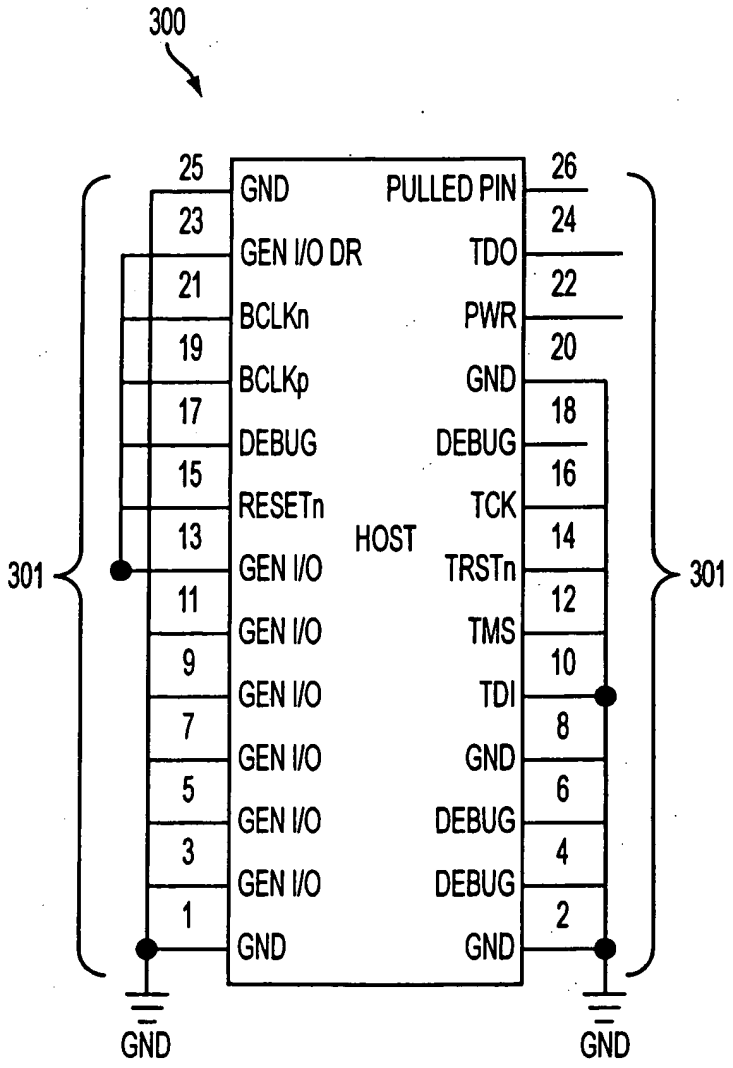
300
25
GND
PULLED PIN
26
23
GEN I/O DR
TDO
24
21
BCLKn
PWR
22
19
BCLKp
GND
20
17
DEBUG
DEBUG
18
15
RESETn
TCK
16
13
HOST
14
301
GEN I/O
TRSTn
301
11
GEN I/O
TMS
12
9
GEN I/O
TDI
10
7
GEN I/O
GND
8
5
GEN I/O
DEBUG
6
3
GEN I/O
DEBUG
4
1
GND
GND
2
GND
GND

FIG. 3

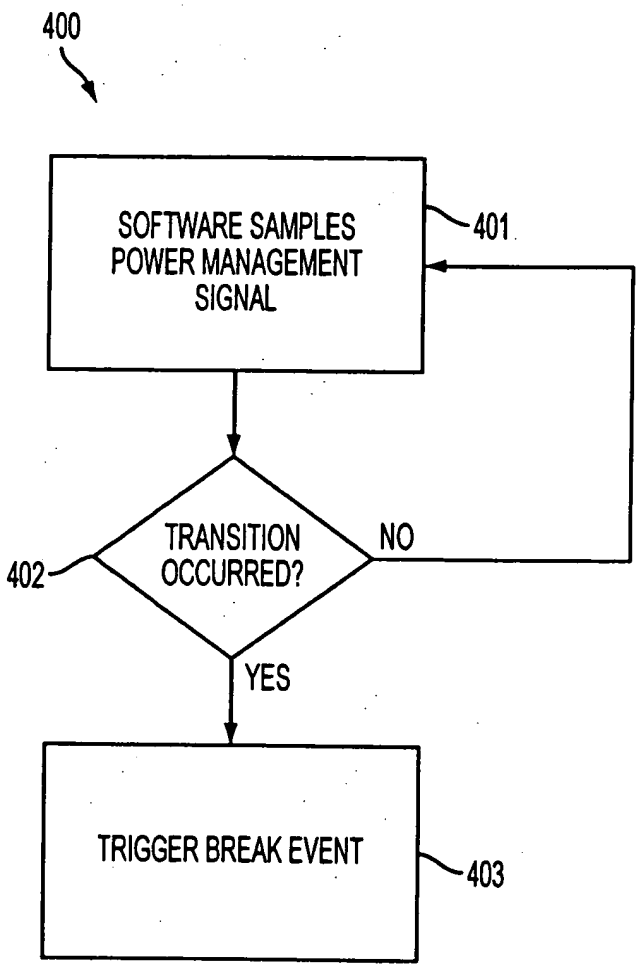
400
SOFTWARE SAMPLES POWER MANAGEMENT SIGNAL
401
TRANSITION OCCURRED?
402
NO
YES
TRIGGER BREAK EVENT
403

FIG. 4

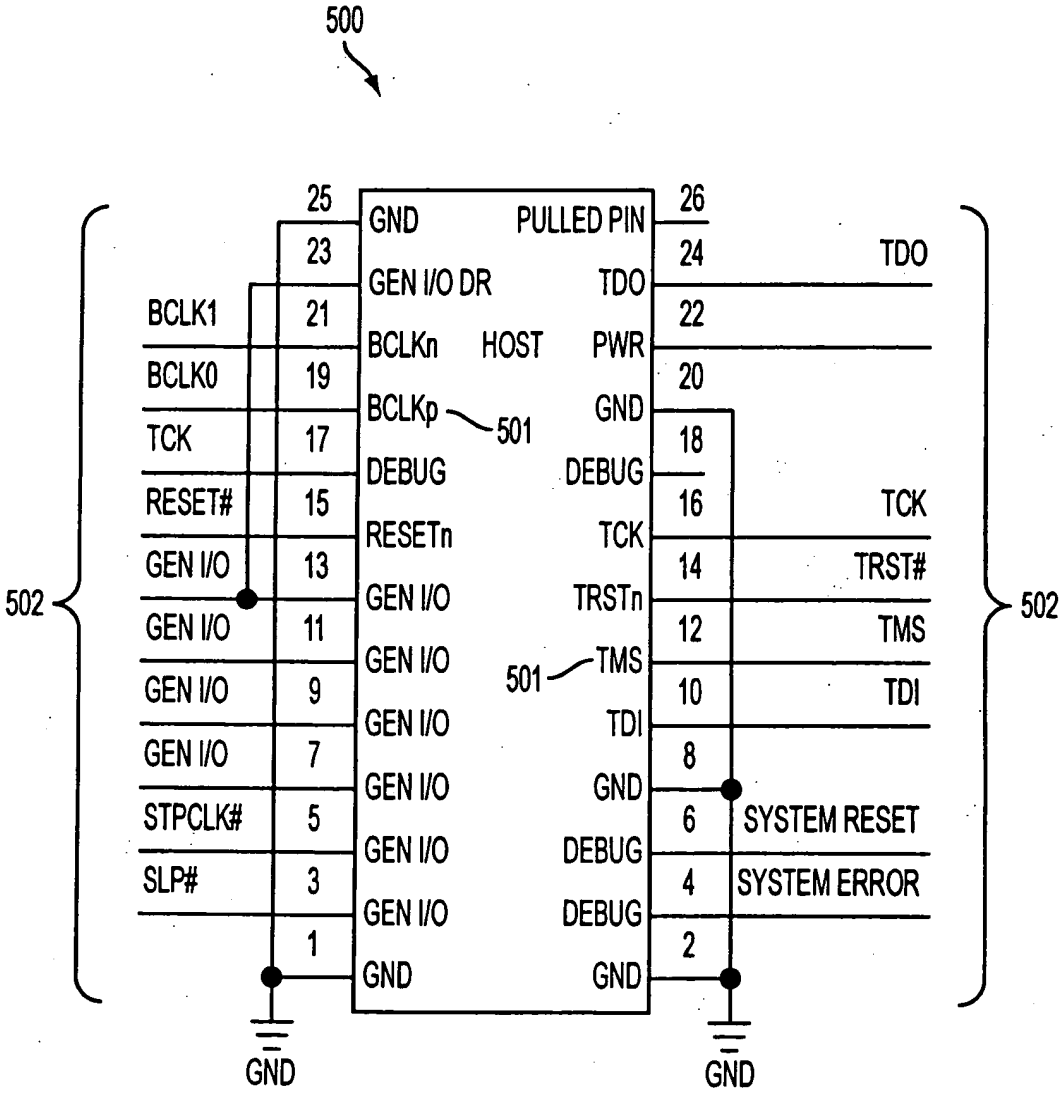
500
502
502
501
501
25
23
21
19
17
15
13
11
9
7
5
3
1
26
24
22
20
18
16
14
12
10
8
6
4
2
GND
PULLED PIN
GEN I/O DR
TDO
BCLKn
HOST
PWR
BCLKp
GND
DEBUG
DEBUG
RESETn
TCK
GEN I/O
TRSTn
GEN I/O
TMS
GEN I/O
TDI
GEN I/O
GND
GEN I/O
DEBUG
GEN I/O
DEBUG
GND
GND
BCLK1
BCLK0
TCK
RESET#
GEN I/O
GEN I/O
GEN I/O
GEN I/O
STPCLK#
SLP#
TDO
TCK
TRST#
TMS
TDI
SYSTEM RESET
SYSTEM ERROR
GND
GND

FIG. 5

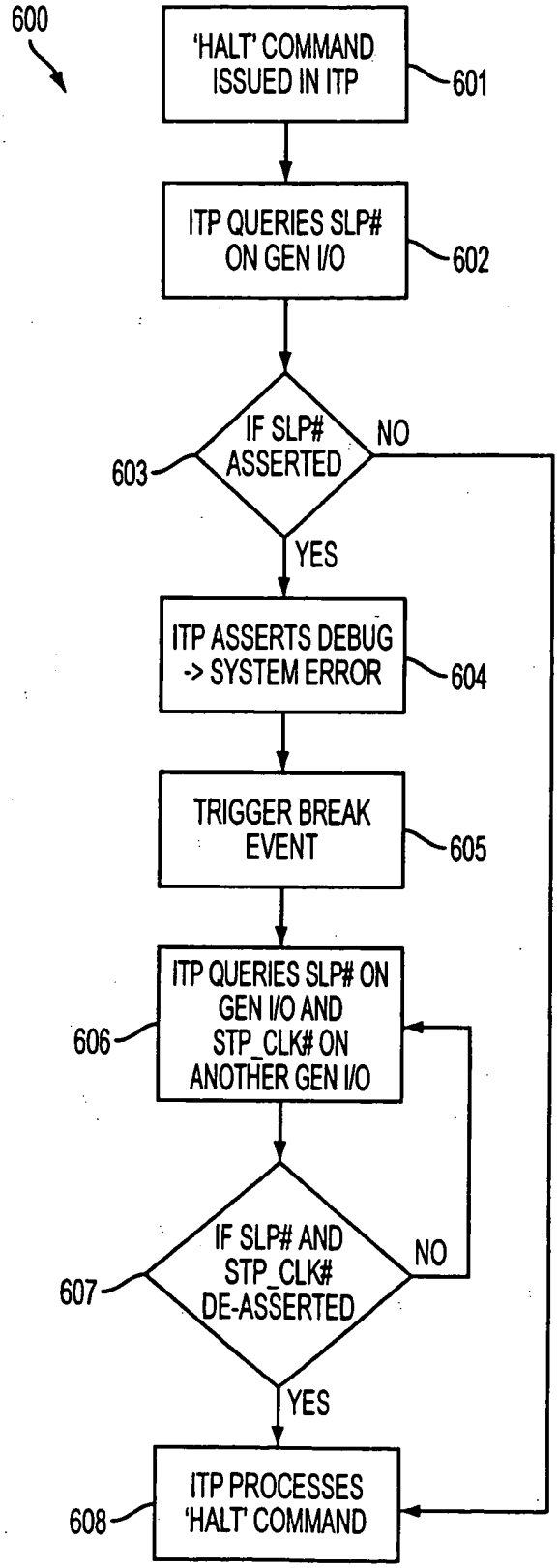
600
'HALT' COMMAND ISSUED IN ITP
601
ITP QUERIES SLP# ON GEN I/O
602
IF SLP# ASSERTED
603
NO
YES
ITP ASSERTS DEBUG -> SYSTEM ERROR
604
TRIGGER BREAK EVENT
605
ITP QUERIES SLP# ON GEN I/O AND STP_CLK# ON ANOTHER GEN I/O
606
IF SLP# AND STP_CLK# DE-ASSERTED
607
NO
YES
ITP PROCESSES 'HALT' COMMAND
608

FIG. 6

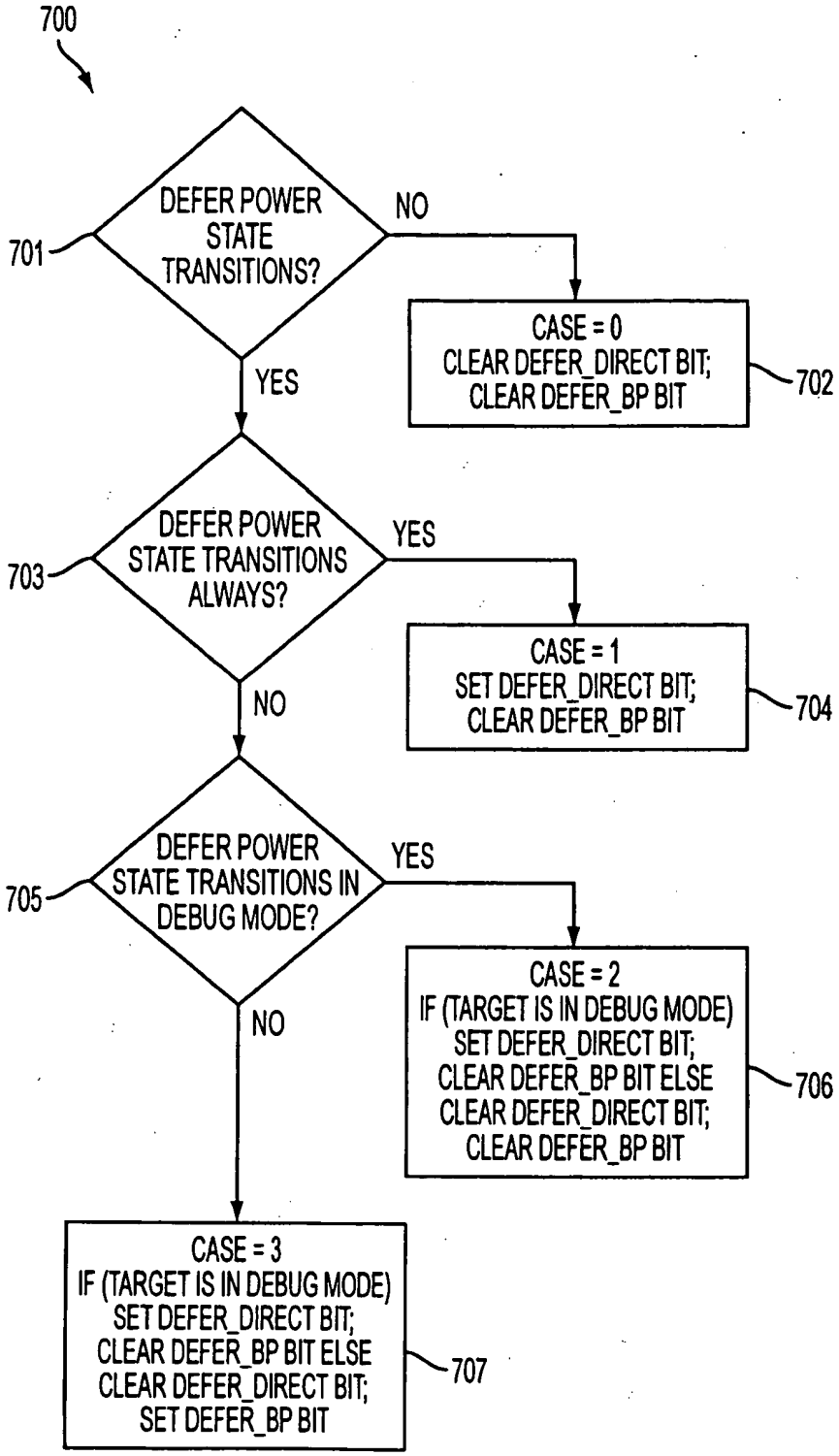
700
DEFER POWER STATE TRANSITIONS?
701
NO
CASE = 0
CLEAR DEFER_DIRECT BIT;
CLEAR DEFER_BP BIT
702
YES
DEFER POWER STATE TRANSITIONS ALWAYS?
703
YES
CASE = 1
SET DEFER_DIRECT BIT;
CLEAR DEFER_BP BIT
704
NO
DEFER POWER STATE TRANSITIONS IN DEBUG MODE?
705
YES
CASE = 2
IF (TARGET IS IN DEBUG MODE)
SET DEFER_DIRECT BIT;
CLEAR DEFER_BP BIT ELSE
CLEAR DEFER_DIRECT BIT;
CLEAR DEFER_BP BIT
706
NO
CASE = 3
IF (TARGET IS IN DEBUG MODE)
SET DEFER_DIRECT BIT;
CLEAR DEFER_BP BIT ELSE
CLEAR DEFER_DIRECT BIT;
SET DEFER_BP BIT
707

FIG. 7

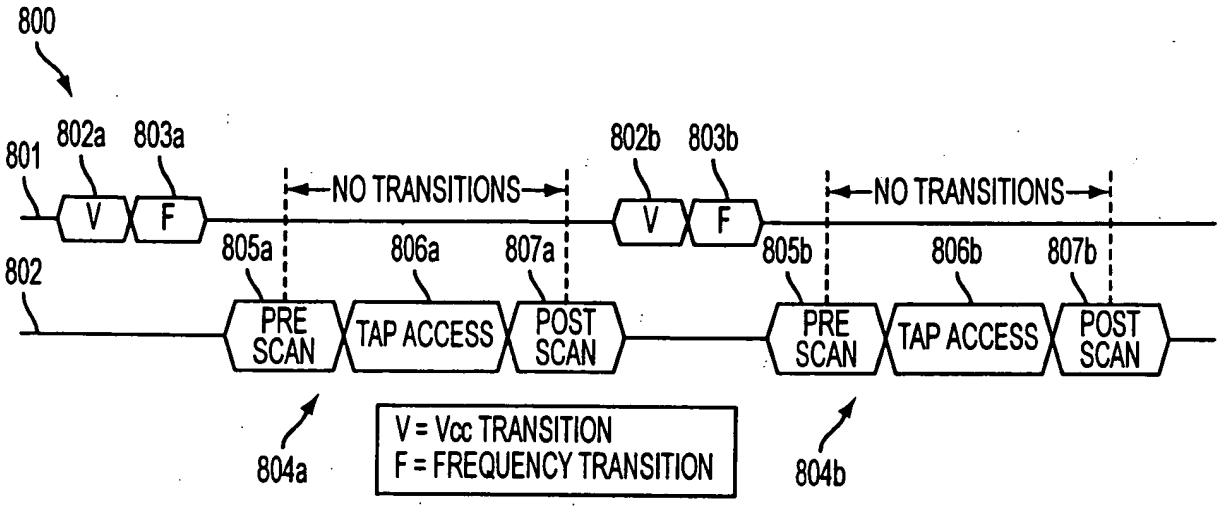
800
801
802a
803a
802b
803b
NO TRANSITIONS
NO TRANSITIONS
V
F
V
F
802
805a
806a
807a
805b
806b
807b
PRE SCAN
TAP ACCESS
POST SCAN
PRE SCAN
TAP ACCESS
POST SCAN
804a
V = Vcc TRANSITION
F = FREQUENCY TRANSITION
804b

FIG. 8

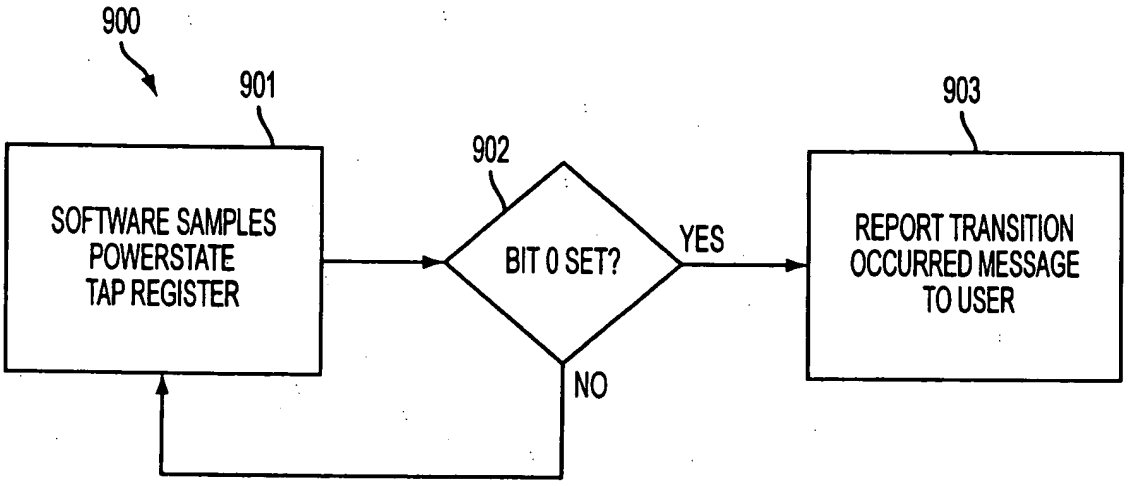
900
901
902
903
SOFTWARE SAMPLES POWERSTATE TAP REGISTER
BIT 0 SET?
YES
NO
REPORT TRANSITION OCCURRED MESSAGE TO USER

FIG. 9

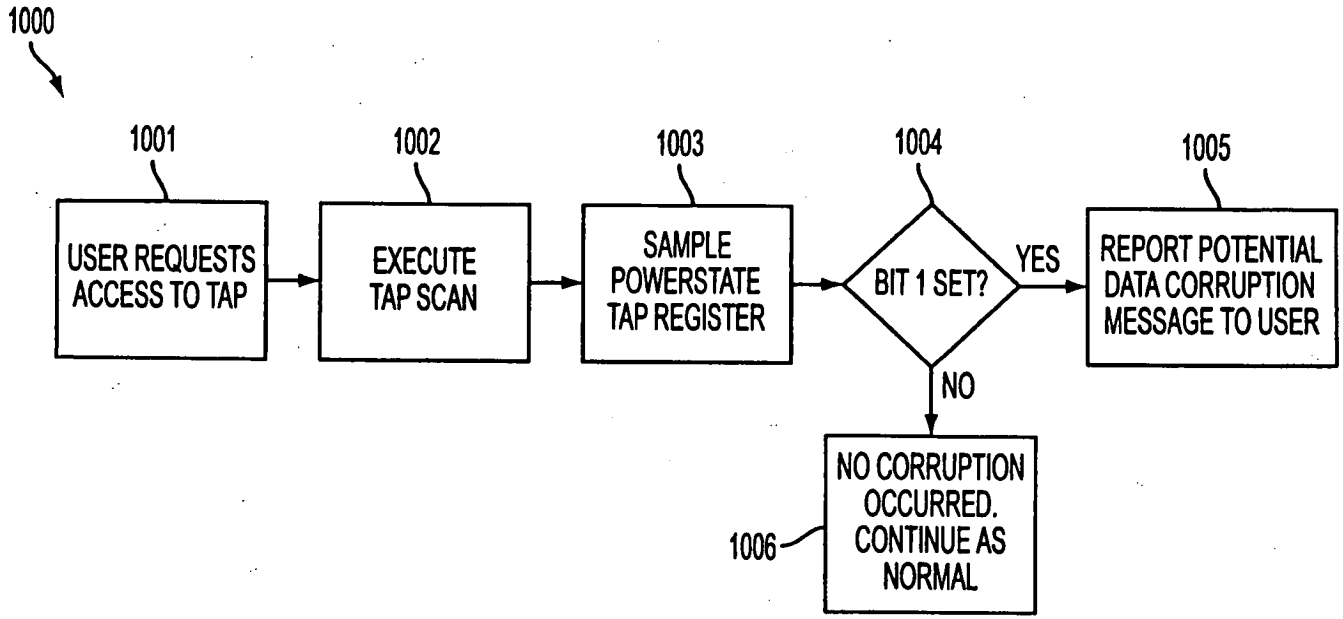
1000
1001
USER REQUESTS ACCESS TO TAP
1002
EXECUTE TAP SCAN
1003
SAMPLE POWERSTATE TAP REGISTER
1004
BIT 1 SET?
YES
1005
REPORT POTENTIAL DATA CORRUPTION MESSAGE TO USER
NO
1006
NO CORRUPTION OCCURRED. CONTINUE AS NORMAL

FIG. 10

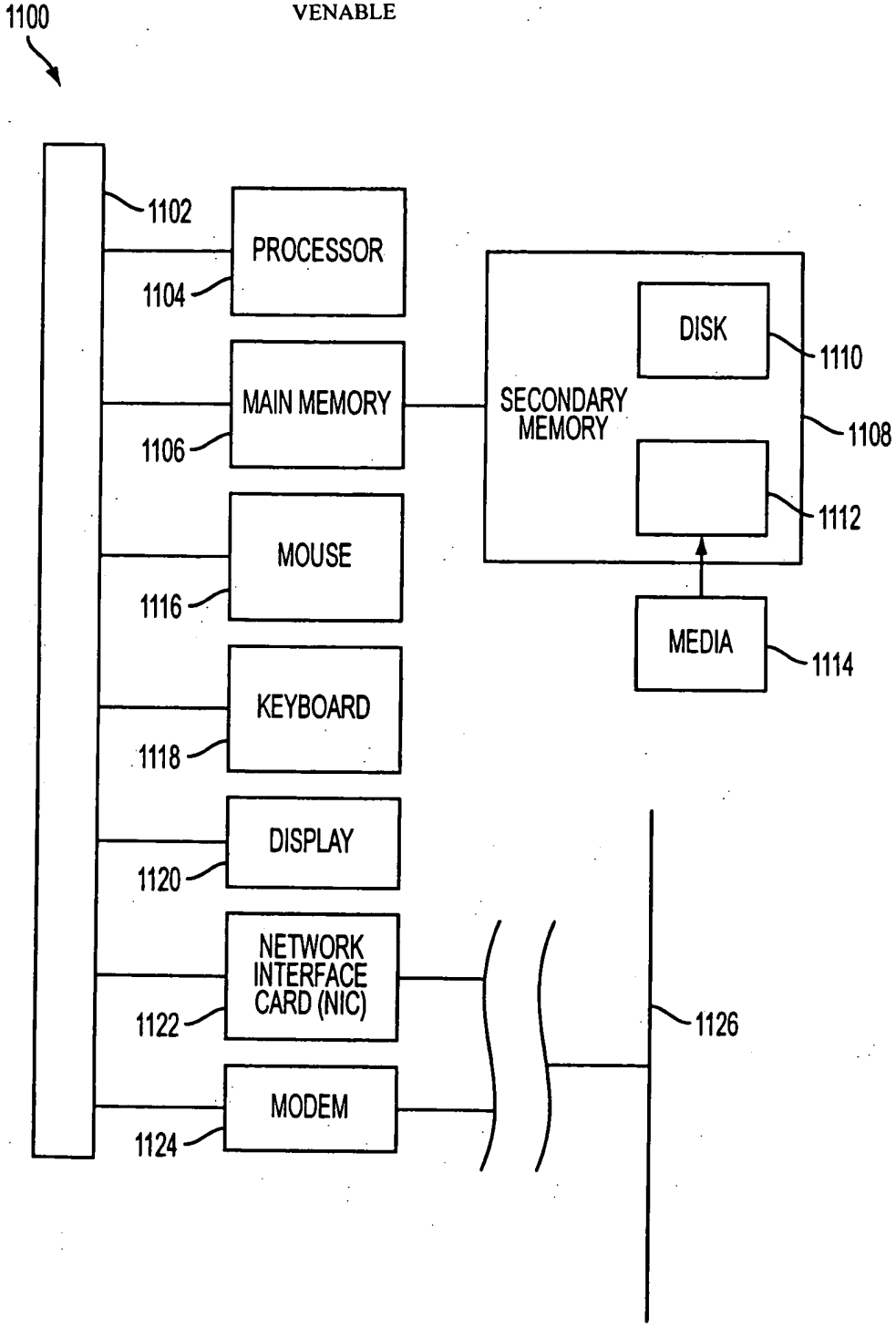
1100
1102
PROCESSOR
1104
MAIN MEMORY
1106
MOUSE
1116
KEYBOARD
1118
DISPLAY
1120
NETWORK INTERFACE CARD (NIC)
1122
MODEM
1124
1126
SECONDARY MEMORY
DISK
1110
1108
1112
MEDIA
1114

FIG. 11

PIN NUMBER	HOST PIN NAME	HOST PIN DESCRIPTION	JTAG/TAP? (Y/N)
1	GND	GROUND	N
2	GND	GROUND	N
3	GEN I/O	DATA TRANSMISSION	N
4	DEBUG	DEBUG	N
5	GEN I/O	DATA TRANSMISSION	N
6	DEBUG	DEBUG	N
7	GEN I/O	DATA TRANSMISSION	N
8	GND	GROUND	N
9	GEN I/O	DATA TRANSMISSION	N
10	TDI	TEST DATA IN	Y
11	GEN I/O	DATA TRANSMISSION	N
12	TMS	TEST MODE SELECT	Y
13	GEN I/O	DATA TRANSMISSION	N
14	TRSTn	TEST LOGIC RESET	Y
15	RESETn	RESET	N
16	TCK	TEST CLOCK	Y
17	DEBUG	DEBUG	N
18	DEBUG	DEBUG	N
19	BCLKp	BUS CLOCK	N
20	GND	GROUND	N
21	BCLKn	BUS CLOCK	N
22	PWR	POWER	N
23	GEN I/O	DRIVES GEN I/O	N
24	TDO	TEST DATA OUT	Y
25	GND	GROUND	N
26	PULLED PIN	PULLED PIN	N

FIG. 12

PIN NUMBER	HOST PIN NAME	TARGET PIN NAME	TARGET PIN DESCRIPTION
1	GND	GND	GROUND
2	GND	GND	GROUND
3	GEN I/O	SLP#	SLEEP STATE
4	DEBUG	SYSTEM ERROR	SYSTEM ERROR
5	GEN I/O	STPCLK#	STOP CLOCK
6	DEBUG	SYSTEM RESET	SYSTEM RESET
7	GEN I/O	GEN I/O	DATA TRANSMISSION
8	GND	GND	GROUND
9	GEN I/O	GEN I/O	DATA TRANSMISSION
10	TDI	TDI	TEST DATA IN
11	GEN I/O	GEN I/O	DATA TRANSMISSION
12	TMS	TMS	TEST MODE SELECT
13	GEN I/O	GEN I/O	DATA TRANSMISSION
14	TRSTn	TRST#	TEST RESET
15	RESETn	RESET#	RESET
16	TCK	TCK	TEST CLOCK
17	DEBUG	TCK	TEST CLOCK
18	DEBUG		
19	BCLKp	BCLK0	BUS CLOCK
20	GND	GND	GROUND
21	BCLKn	BCLK1	BUS CLOCK
22	PWR	PWR	POWER
23	GEN I/O DR	GEN I/O DR	DRIVES GEN I/O
24	TDO	TDO	TEST DATA OUT
25	GND	GND	GROUND
26	PULLED PIN	PULLED PIN	GROUND

FIG. 13